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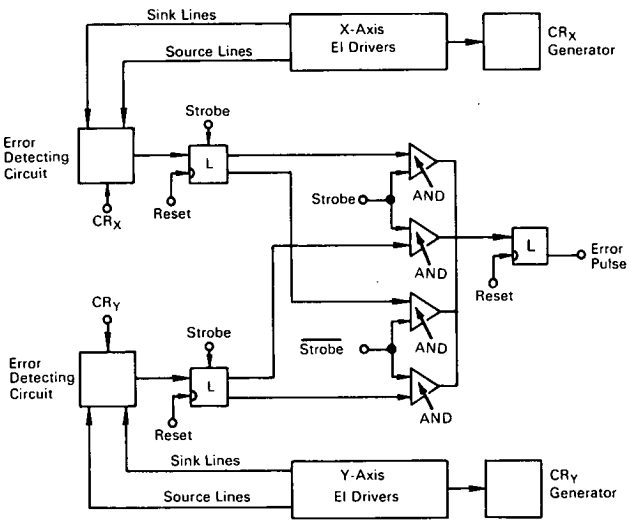
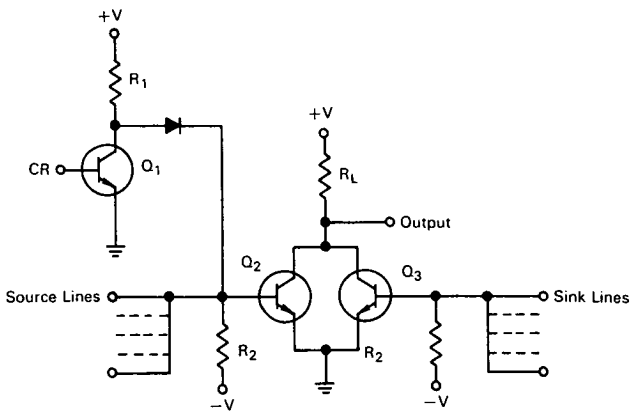
NASA TECH BRIEF

Circuit Detects Errors in Address Currents for Magnetic Core Arrays





The problem: Error detection in voltage source (E)-current sink (I) half-select addressing of magnetic core memory arrays. In such a system each EI pair drives a discrete half-select line in the memory. All combinations of EI pairs are employed. Thus half-select addressing is accomplished by discretely actuating one voltage source circuit and one current source circuit. Any of the following conditions can introduce output errors in this system: address without voltage source, without current sink, or without voltage source-current sink; address with multiple sources and single sink, with single source and multiple sinks, or with multiple sources and sinks; or address out-of-time (transient addressing).

The solution: An address current error detector that generates a signal whenever any of the error-producing conditions arise.

How it's done: As indicated in the block diagram of the system, an error detecting circuit is provided for each addressing coordinate. The outputs of all the voltage sources and current sinks plus the coordinate address clock (CR, i.e., CR_x or CR_y) pulse are monitored by the associated error detecting circuit. If one source and one sink circuit are actuated when the current address clock pulse is present, no signal is generated by the error detecting circuit. However, if any other combination of sources, sinks, and the coordinate address clock pulse (present or absent) is impressed upon the error detecting circuit, it generates a signal that is processed by latch circuits and AND gates to present an error pulse at the output of the error detection system.

Details of the error detecting block are shown in the circuit diagram. In the absence of a CR pulse and any

(continued overleaf)

source or sink signal, transistor Q_2 is saturated; as a result, the bias current through R_1 and the output level are down. When only a CR pulse is present, Q_2 turns off, and the output level is up. In this case, a single source signal and a single sink signal will not override the back bias through the resistors R_2, and the output remains up. If two or more source signals are present, Q_2 turns on and the output level is down. If two or more sink signals are present, Q_3 turns on, and the output level is down. The CR pulse is not generated unless one source signal and one sink signal are present. Thus, during the time of a strobe signal at the AND gates, an up level on the output indicates error-free operation and a down level indicates erroneous operation.

Notes:

1. The error detection system is compatible with most memory configurations employing source-sink addressing or driver-gate addressing. It may also have application in test equipment to determine signal coincidence.
2. Inquiries concerning this innovation may be directed to:

   Technology Utilization Officer
   Marshall Space Flight Center
   Huntsville, Alabama, 35812
   Reference: B65-10047

Patent status: NASA encourages commercial use of this innovation. No patent action is contemplated.

Source: International Business Machines Corporation, under contract to Marshall Space Flight Center (M-FS-234)